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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,632	11/13/2000	Alexander L. Minkin	019680-00200US	3726

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EXAMINER

QUILLEN, ALLEN E

ART UNIT	PAPER NUMBER
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2676

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/712,632

Applicant(s)

MINKIN

Examiner

Allen E. Quillen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Drawings

1. New corrected drawings are required in this application because they do not meet the requirements of MPEP 608.02, 37 CFR 1.84. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

Content of Specification

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

The application lacks specificity to the related applications (page 1, line 5; page 12, line 26).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined

was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Van Hook, et al, U.S. Patent 6,353,438.

4. Regarding claim 1, representative of claim 14, Van Hook discloses a method of storing a texel in a texel cache comprising: reading a t coordinate of the texel, the t coordinate comprising a plurality of bits; reading a s coordinate of the texel, the s coordinate comprising a plurality of bits; and forming an offset by concatenating bits of the t coordinate with bits of the s coordinate (Figures 7, 11, 12, 13, Columns 1, lines 48-55, Column 2, lines 20-27; Column 3, lines 17-26; Column 7, line 1-12; non-contiguous storage locations, Column 8, line 64 through Column 9, line 1-5; Column 11, line 1-4; Column 12, lines 5-11).

5. Regarding claim 2, Van Hook discloses the method of claim 1 further comprising forming an index by concatenating bits of the t coordinate with bits of the s coordinate (Column 7, line 26).

6. Regarding claim 3, Van Hook discloses the method of claim 2 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements (see above; Column 7, line 9-11).

7. Regarding claim 4, Van Hook discloses the method of claim 3 further comprising storing the texel in a storage element identified by the offset (see above; Column 8, line 64 through Column 9, line 5).

8. Regarding claim 5, Van Hook discloses the method of claim 4 further comprising storing the texel in a cache line identified by the index (see above; Column 7, lines 4-34).

9. Regarding claim 6, Van Hook discloses the method of claim 5 wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating the lower bits of the t coordinate with the lower order bits of the s coordinate (Column 11, lines 1-4; Column 13, lines 36-62).

10. Regarding claim 7, Van Hook discloses the method of claim 6 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory (Column 1, line 40 through Column 2, lines 67).

11. Regarding claim 8, Van Hook discloses the method of claim 7 further comprising forming a tag by concatenating the high order bits of the s coordinate and high order bits of the t coordinate, adding the address in main memory, and storing the tag in a look-up table (Figure 9, Column 7, line 21).

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12. Regarding claim 9, Van Hook discloses the method of claim 8 wherein the forming an index by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating middle order bits of the t coordinate with middle order bits of the s coordinate (Column 7, lines 30-34).

13. Regarding claim 10, representative of claim 15, Van Hook discloses the method of claim 1 wherein the texel is associated with a MIPmap having a level of detail (*resolution*, Column 1, lines 45-60; Column 4, line 26) comprising a plurality of bits, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the level of detail (see above; Column 4, lines 15, 36;

14. Regarding claim 11, representative of claim 16, Van Hook discloses the method of claim 1 wherein the texel is associated with a texture having a texture identification comprising a plurality of bits, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the texture identification (see above; texture mapping, Column 2, lines 6-35; Column 14, lines 39-64)

15. Regarding claim 12, representative of claim 18, Van Hook discloses the method of claim 1 wherein the texel is associated with a texture having an r coordinate comprising at least one bit, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the r coordinate (see

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above; *3D, trilinear filtering, RGB, depth cueing*, Column 1 line 45 through Column 2, line 60; Column 15, lines 8-11; 34-35).

16. Regarding claim 13, representative of claim 17, Van Hook discloses the method of claim 1 wherein the texel has a main memory address comprising a plurality of bits, further comprising forming an index signal by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the main memory address (see above; Column 16, line 38-43).

17. Regarding claim 19, representative of claims 20-25, Van Hook discloses a method of generating a texture cache address comprising: reading an s coordinate of a texture, wherein the s coordinate comprises a plurality of bits; passing lower order bits of the s coordinate as a portion of an offset; passing middle order bits of the s coordinate as a portion of an index; and passing high order bits of the s coordinate as a portion of a tag (see above; Column 7, lines 1-50).

18. Regarding claim 26, Van Hook discloses a method of storing address information for a group of texels comprising: storing an index and offset of a first texel; and storing a line index of at least one of the other quad of texels, wherein the stored address information comprises information necessary to determine a group of addresses in a texture cache (see above; Figures 9 and 14; Column 9, line 55; Column 10, line 38; Column 12, lines 14-48).

19. Regarding claim 27, Van Hook discloses the method of claim 26 wherein the texture cache comprises a plurality of cache lines, further comprising storing an indication of which cache lines need to be updated (see above; Column 12, lines 33-41).

20. Regarding claim 28, Van Hook discloses the method of claim 27 further comprising storing information as to the wrap mode used to store the group of texels in the texel cache (Column 12, lines 15-67).

21. Regarding claim 29, Van Hook discloses a graphics processor comprising: a graphics pipeline coupled to receive texels and provide s and t coordinates and a memory address; a cache address generator, coupled to receive the s and t coordinates and the memory address, and configured to generate an offset, an index, and a tag using the s and t coordinates and the memory address, and a cache unit, coupled to provide texels, and receive the offset, index and tag, wherein the cache unit further comprises a texture cache (see above; Figure 9, element 903, Column 7, line 4-34; Column 10, lines 8-34).

22. Regarding claim 30, representative of claim 32, Van Hook discloses a computer system comprising: a central processing unit (CPU); a main memory coupled to the CPU; and a graphics processor as set forth in claim 29, coupled to the CPU (Figure 10, elements 1017, 1012, 1015, 1030; Columns 17, line 45 through Column 18, line 62).

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23. Regarding claim 31, Van Hook discloses a graphics processor comprising: a texture cache manager, coupled to receive texel addresses and provide a packet of data, and a fetch request; a memory controller coupled to receive the fetch request and provide a cache line update; a FIFO coupled to receive and provide packets, and configured to store a plurality of packets; and a texture cache controller coupled to receive data stored in cache lines, wherein the packets comprise an offset of a first texel, an index of a first texel, and information required to generate an offset and an index of a second texel (see above; Column 15, line 1 through Column 17, line 44) .

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

February 10, 2003



**MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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